REMARKS

Applicant would like to thank the examiner for indicating that claims 10 and 23 include allowable subject matter and would be allowable if rewritten in independent form.

Drawings

The Patent Office objected to Figure 2 under 37 C.F.R. § 1.83(a). More specifically, the Patent Office stated that the "node connected between transistor (Q1) and BIASING NETWORK (66)" must be shown or the features cancelled from the claims. Applicant would like to thank Examiner Nguyen for the telephone call on March 29, 2005 during which he clarified that the objection was given because there was no "dot" or "node" connecting resistor $R1_1$, $C1_1$, and $C2_1$ to the base of transistor (Q1) and no "dot" or "node" connecting resistor $R1_N$, $C1_N$, and $C2_N$ to the base of transistor (QN). Applicant has amended Figure 2 to include "dots" or "nodes" more clearly showing the connection between resistor $R1_1$, $C1_1$, and $C2_1$ and the base of transistor (Q1) and the connection between resistor $R1_N$, $C1_N$, and $C2_N$ and the base of transistor (QN). Accordingly, the objection to Figure 2 under 37 C.F.R. § 1.83(a) should be withdrawn.

Claim Objections

The Patent Office objected to claims 12 and 25 because of informalities. More specifically, the Patent Office stated that "output matching circuitry" should be corrected to "output matching network" in claims 12 and 25. Claims 12 and 25 have been amended as suggested by the Patent Office. Thus, the objection to claims 12 and 25 should be withdrawn.

§ 112

The Patent Office rejected claims 7, 9, 11, 20, 22, and 24 under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Regarding claims 7, 9, 20, and 22, the Patent Office stated that a "bias network coupled to the input of transistor (Q1) of Figure 2 is not shown, since there is no 'node' coupled between 'bias network' and transistor (Q1)." As stated above, Applicant has amended Figure 2 to include "dots" or "nodes" showing the connection between resistor $R1_1$, $C1_1$, and $C2_1$ and the base of transistor (Q1) and the connection between resistor $R1_N$, $C1_N$, and $C2_N$ to the base of transistor

(QN). Thus, Figure 2 clearly illustrates that the inputs, or bases, of the transistors (Q1-QN) are coupled to the bias network (66) via resistors ($R1_1$-$R1_N$), respectively. It should also be noted that claims 7, 9, 20, and 22 do not use the language "bias network coupled to the input of transistor (Q1)." For example, claim 7 reads, in pertinent part, "a bias network adapted to provide a bias signal to the input of each of the transistors in the array of transistors based on a power control signal." Since Figure 2 clearly illustrates that the inputs, or bases, of the transistors (Q1-QN) are coupled to the bias network (66) via resistors ($R1_1$-$R1_N$), respectively, claims 7, 9, 20, and 22 are definite and therefore allowable.

Regarding claims 11 and 24, the Patent Office stated that there is insufficient antecedent basis for "the wideband power amplifier." Applicant has amended claims 11 and 24 to replace "the wideband power amplifier" with "the array of transistors." As such, claims 11 and 24 are allowable.

§ 102

The Patent Office rejected claims 1-6, 8, 12-19, 21, 25, and 26 under 35 U.S.C. § 102(e) as being anticipated by Steel (U.S. Patent No. 6,658,265). "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 UPPQ 2d 1051, 1053 (Fed. Cir. 1987).*

Regarding claim 1, Steel fails to expressly or inherently disclose at least a first matching circuit coupling the first input node to the inputs of each transistor in the array of transistors, and a second matching circuit coupling the second input node to the inputs of each transistor in the array of transistors. As illustrated in Figure 2 and discussed in paragraph [00223] of Applicant's specification, the capacitors ($C1_1$-$C1_N$) and inductor (L1) form a first matching circuit, and the capacitors ($C2_1$-$C2_N$) and inductor (L2) form a second matching circuit. The first matching circuit ($C1_1$-$C1_N$ and L1) couples the first input node (A) to the inputs, or bases, of each of the transistors (Q1-QN). More specifically, the first input node (A) is coupled to the input of the first transistor (Q1) via capacitor ($C1_1$), and the first input node (A) is coupled to the input of the Nth transistor (QN) via capacitor ($C1_N$). In a similar fashion, the second matching circuit ($C2_1$-$C2_N$ and L2) couples the second input node (B) to the inputs, or bases, of each of the transistors (Q1-QN). More specifically, the second input node (B) is coupled to the input of the first

transistor (Q1) via capacitor ($C2_1$), and the second input node (B) is coupled to the input of the Nth transistor (QN) via capacitor ($C2_N$).

Referring to Figure 3, Steel discloses first and second matching networks (N1 and N2). The first matching network (N1) only couples the GSM frequency band to the transistor (Q1). The second matching network (N2) only couples the DCS frequency band to the transistor (Q4). So, even if the transistors (Q1, Q4) are interpreted as the claimed "array of transistors," the first matching network (N1) does not couple the GSM frequency band to the input of each transistor in the array of transistors. In other words, the first matching network does not couple the GSM frequency band to the inputs of each of the transistors (Q1 and Q4). In a similar fashion, the second matching network (N2) does not couple the DCS frequency band to the input of each of the transistors (Q1 and Q4). Accordingly, Steel fails to expressly or inherently disclose at least a first matching circuit coupling the first input node to the inputs of each transistor in the array of transistors and a second matching circuit coupling the second input node to the inputs of each transistor in the array of transistors. Thus, claim 1 is allowable.

For at least the same reasons claim 1 is allowable, claims 2-6, 8, 12, and 13 are also allowable. However, Applicant reserves the right to further address the rejections of clams 2-6, 8, 12, and 13 in the future if necessary.

Regarding claim 14, in view of the discussion of claim 1, Steel fails to expressly or inherently disclose a plurality of matching circuits each coupling a corresponding one of the plurality of input nodes to the inputs of each transistor in the array of transistors. As such claim 14 is allowable.

For at least the same reasons claim 14 is allowable, claims 15-19, 21, 25, and 26 are also allowable. However, Applicant reserves the right to further address the rejections of clams 15-19, 21, 25, and 26 in the future if necessary.

Conclusion

In view of the discussion above, claims 1-26 are allowable. Reconsideration is respectfully requested. If any issues remain, the examiner is encouraged to contact the undersigned attorney of record to expedite allowance and issue.

Respectfully submitted,

WITHROW & TERRANOVA, P.L.L.C.

By:

Benjamin S. Withrow
Registration No. 40,876
P.O. Box 1287
Cary, NC 27512
Telephone: (919) 654-4520

Date: March 30, 2005
Attorney Docket: 2867-193

CERTIFICATE OF MAILING

I HEREBY CERTIFY THAT THIS DOCUMENT IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS FIRST-CLASS MAIL, IN AN ENVELOPE ADDRESSED TO: **MAIL STOP AMENDMENT, COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450**, ON MARCH 30, 2005.

Kelly Farrow
Name of Depositor

Signature

3/30/05
Date of Signature

In the Drawings:

Please find enclosed herewith a replacement sheet for Figure 2.